NON-VOLATILE PRODUCT TERM (PTERM) CELL

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FIELD OF THE INVENTION

[0001] The present invention relates to a method and structure for configuring a programmable logic device. More specifically, the present invention relates to an improved product term (pterm) cell, which replaces SRAM cells with non-volatile embedded electrically erasable (EE) memory cells.

RELATED ART

[0002] Conventional complex programmable logic devices (CPLDs), such as the COOLRUNNER™ family of CPLDs available from Xilinx, Inc., include a basic circuit block known as a product term (pterm) cell.

[0003] Conventional CPLD designs require a power-up initialization cycle. During this cycle, the contents of a non-volatile memory, such as an electrically erasable memory array, are transferred into a plurality of SRAM latches embedded in a logic core. This transfer typically occurs over a plurality of memory cycles, on an address-by-address basis. For example, a conventional CPLD may include an electrically erasable memory array that stores about 150,000 configuration values, which are loaded into corresponding latches 1500 bits at a time. Thus, 100 transfers must be made from the electrically erasable memory array to the latches in order to configure the CPLD. Once the configuration values are stored in the latches, the latches configure the logic core to implement a user-defined application.

[0004] Two drawbacks of a conventional initialization cycle are the complex circuitry required to transfer the configuration values from the electrically erasable memory

array to the latches, and the relatively long time required to transfer the configuration values from the electrically erasable array to the latches. In addition, the conventional initialization process is subject to disruption from noise and variations in the power supply voltage.

[0005] It would therefore be desirable to have an improved product term cell for use in a CPLD.

SUMMARY

[0006] Accordingly, present invention provides a non-volatile product term cell having a smaller layout area than a conventional SRAM product term (pterm) cell, thereby resulting in a reduced die size. Moreover, the non-volatile pterm cell of the present invention directly applies a configuration state to the product term elements, without the need to transfer information from an electrically erasable memory cell to associated SRAM cells.

[0007] In accordance with one embodiment, the non-volatile product term cell includes a first floating gate element which forms part of a first p-channel floating gate transistor and part of a first n-channel floating gate transistor. The product term cell also includes a second floating gate element which forms part of a second p-channel floating gate transistor and part of a second n-channel floating gate transistor. A control gate is capacitively coupled to both the first and second floating gate elements. In addition, a first tunnel oxide capacitor is coupled to the first floating gate element, and a second tunnel oxide capacitor is coupled to the second floating gate element.

[0008] The sources of the first and second p-channel transistors are commonly coupled to a first voltage supply terminal, and the sources of the first and second n-channel

transistors are commonly coupled to a ground supply voltage terminal. A first transistor pair, including a p-channel transistor and an n-channel transistor, is coupled between the drain of the first p-channel transistor and the drain of the second n-channel transistor. Similarly, a second transistor pair, including a p-channel transistor and an n-channel transistor, is coupled between the drain of the second p-channel transistor and the drain of the first n-channel transistor.

[0009] The first and second floating gate elements are erased by applying a high positive voltage to the control gate, grounding the tunnel oxide capacitors, and allowing the first voltage supply terminal to float. When the first floating gate element is erased, the first p-channel floating gate transistor is enabled (turned on) and the first n-channel floating gate transistor is disabled (turned off). Similarly, when the second floating gate element is erased, the second p-channel floating gate transistor is enabled and the second n-channel floating gate transistor is disabled.

[0010] The first and/or second floating gate elements can then be programmed, if desired, by applying a high positive voltage to the tunnel oxide capacitor(s) and the ground supply voltage to the control gate. When the first floating gate element is programmed, the first p-channel floating gate transistor is disabled and the first n-channel floating gate transistor is enabled. Similarly, when the second floating gate element is programmed, the second p-channel floating gate transistor is disabled and the second n-channel floating gate transistor is enabled.

[0011] An input signal (Z_{IN}) is applied to the gates of the transistors of the first transistor pair, and the complement of the input signal ($Z_{IN\#}$) is applied to the gates of the

transistors of the second transistor pair. An output signal is provided at the common drain regions of the first and second transistor pairs in response to the input signal and the programmed/erased states of the first and second floating gate elements.

[0012] If the first and second floating gate elements are both erased, then the output signal is pulled up to the first supply voltage by either the first or second p-channel transistor (depending on the state of the input signal $Z_{IN}/Z_{IN\#}$). If the first and second floating gate elements are both programmed, then the output signal is pulled down to the ground supply voltage by either the first or second n-channel transistor (depending on the state of the input signal $Z_{IN}/Z_{IN\#}$). If the first floating gate element is erased and the second floating gate element is programmed, then the output signal is either pulled up to the first supply voltage by the first p-channel floating gate transistor, or pulled down to the ground supply voltage by the second n-channel floating gate transistor (depending on the state of the input signal Z_{IN}). Similarly, if the second floating gate element is erased and the first floating gate element is programmed, then the output signal is either pulled up to the first supply voltage by the second p-channel floating gate transistor, or pulled down to the ground supply voltage by the first n-channel floating gate transistor (depending on the state of the complementary input signal $Z_{IN\#}$).

[0013] In an alternate embodiment, the sources of the first and second n-channel floating gate transistors are coupled to first and second bit lines, respectively. In this embodiment, a read transistor is coupled between the output terminal and a voltage supply terminal. When the read transistor is enabled, the programmed/erased states of the first and second floating

gate elements can be determined by monitoring the first and second bit lines.

[0014] The present invention will be more fully understood in view of the following description and drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0015] Fig. 1 is a circuit diagram of a product term cell in accordance with one embodiment of the present invention.

[0016] Fig. 2 is a block diagram of a 3x2 array of product term cells, each of which is substantially identical to the product term cell of Fig. 1.

[0017] Fig. 3 is a circuit diagram of a product term cell in accordance with another embodiment of the present invention.

[0018] Fig. 4 is a block diagram of a 2x2 array of product term cells, each of which is substantially identical to the product term cell of Fig. 3.

DETAILED DESCRIPTION

[0019] Fig. 1 is a circuit diagram of a symmetrical product term (pterm) cell 100 in accordance with one embodiment of the present invention. Product term cell 100 includes high-voltage p-channel transistors 101-104, n-channel transistors 105-108, capacitors 111-112, and tunnel oxide capacitor elements 121-122.

[0020] A left-side programming bit $PBIT_L$ is applied to a first terminal of tunnel oxide capacitor element 121. In the described embodiment this first terminal of tunnel oxide capacitor element 121 is formed by a conductively doped (e.g., n-type) semiconductor substrate region. A thin oxide layer (e.g., 10 Angstroms) is formed over the first terminal of tunnel oxide capacitor element 121, and a conductively doped

polysilicon floating gate element FG_L is formed over this thin oxide layer, thereby forming the second terminal of tunnel oxide capacitor element 121. In the described embodiment, tunnel oxide capacitor element 121 has a layout area of about 0.16 square microns. However, other sizes are possible in other embodiments.

[0021] The floating gate element FG_L also forms a floating gate electrode of p-channel transistor 101, a floating gate electrode of n-channel transistor 108, and a first plate electrode of capacitor 111.

[0022] Similarly, a right-side programming bit $PBIT_R$ is applied to a first terminal of tunnel oxide capacitor element 122. In the described embodiment, tunnel oxide capacitor element 122 is substantially identical to tunnel oxide capacitor element 121. Tunnel oxide capacitor element 122 includes a conductively doped polysilicon floating gate element FG_R. This floating gate element FG_R also forms a floating gate electrode of p-channel transistor 103, a floating gate electrode of n-channel transistor 106, and a first plate electrode of capacitor 112. The second plate electrodes of capacitors 111 and 112 are coupled to receive a control gate signal CG.

[0023] Each of the high-voltage p-channel transistors 101-104 has a relatively thick gate oxide, which enables these transistors to operate in response to voltages much greater than the nominal supply voltage. For example, if product term cell 100 normally operates in response to a nominal supply voltage of 1.8 Volts, then high-voltage p-channel transistors 101-104 are capable of operating in response to voltages of 12-14 Volts, without adverse effects.

[0024] P-channel transistors 101-102 and n-channel transistors 105-106 are connected in series between a V_{DD}

terminal (which receives a V_{DD} signal) and a ground voltage supply terminal (which is maintained at a ground supply voltage of 0 Volts). Similarly, p-channel transistors 103-104 and n-channel transistors 107-108 are connected in series between the V_{DD} terminal and the ground voltage supply terminal. The n-type body regions of p-channel transistors 101-104 are coupled to the V_{DD} terminal. In the described embodiment, each of transistors 101-108 has a width-to-length ratio of 0.56/0.5. However, these transistors can have other width-to-length ratios in other embodiments.

[0025] The gates of p-channel transistor 102 and n-channel transistor 105 are commonly coupled to a Z_{IN} input terminal (which receives an input signal Z_{IN}). The gates of p-channel transistor 104 and n-channel transistor 107 are commonly coupled to a $Z_{IN\#}$ input terminal (which receives an input signal $Z_{IN\#}$ that is typically the inverse of the input signal Z_{IN}). The drains of transistors 102, 104, 105 and 107 are commonly connected to an output terminal 130, which provides an output signal (OUT). In some embodiments, the $Z_{IN\#}$ input signal may be provided by an inverter coupled between the Z_{IN} and $Z_{IN\#}$ input terminals.

[0026] Product term cell 100 is initially erased as follows. The $PBIT_L$ and $PBIT_R$ signals are connected to receive the ground supply voltage (0 Volts), the V_{DD} terminal is left floating, and the control gate voltage CG is raised to a programming voltage V_{PP} of about 12-14 Volts for about 100 milli-seconds (msec). Under these conditions, electrons travel from the first terminals of tunnel oxide capacitor elements 121 and 122 toward the control gate terminal CG, and are trapped on the left floating gate FG_L and the right floating gate FG_R, respectively. The negative electronic charge on left floating gate FG_L lowers the threshold voltage

of p-channel transistor 101 and raises the threshold voltage of n-channel transistor 108. Similarly, the negative electronic charge on right floating gate FG_R lowers the threshold voltage of p-channel transistor 103 and raises the threshold voltage of n-channel transistor 106.

[0027] Product term cell 100 can then be programmed as follows. The control gate voltage CG is initially raised to ½ the programming voltage V_{PP}, or about 6-7 Volts. The $PBIT_L$ signal is then raised from the ground supply voltage to the programming voltage V_{PP} (12-14 Volts) if the left floating gate FG_L is to be programmed. Similarly, the $PBIT_R$ signal is raised from the ground supply voltage to the programming voltage V_{PP} (12-14 Volts) if the right floating gate FG_R is to be programmed. If neither the left floating gate FG_L nor the right floating gate FG_R is to be programmed, then both the $PBIT_L$ and the $PBIT_R$ signals remain at the ground supply voltage.

[0028] After the $PBIT_L$ and $PBIT_R$ signals have been set, the control gate voltage CG is lowered to the ground supply voltage (0 Volts). At this time, the left floating gate FG_L is programmed if the $PBIT_L$ signal is raised to the programming voltage V_{PP}, and the right floating gate FG_R is programmed if the $PBIT_R$ signal is raised to the programming voltage V_{PP}. During the programming operation, negative electronic charge is removed from the associated floating gate. For example, if the left floating gate FG_L is programmed, negative electronic charge is removed from this floating gate. As a result, the threshold voltage of p-channel transistor 101 is raised, and the threshold voltage of n-channel transistor 108 is lowered. If the $PBIT_L$ (or $PBIT_R$) signal remains at the ground supply voltage, then the associated floating gate FG_L (or FG_R) remains in the erased state, and is not programmed. The program

operation requires approximately 10 msec. When the program operation is complete, the control gate voltage CG is raised back to a voltage of ½ V_{PP}.

[0029] Fig. 2 is a block diagram of a 3x2 array 200 of product term cells 201_1-201_3, 202_1-202_3 each of which is substantially identical to product term cell 100. Although a 3x2 array is illustrated, it is understood that this array can be expanded or contracted as necessary in view of the following teachings. In the illustrated embodiment, the product term cells 201_1-201_3 of the first column are commonly coupled to receive the $PBIT_{L1}$ and $PBIT_{R1}$ signals. Similarly, the product term cells 202_1-202_3 of the second column are commonly coupled to receive the $PBIT_{L2}$ and $PBIT_{R2}$ signals. Each row of product term cells 201_1-202_1, 201_2-202_2, and 201_3-202_3 is coupled to receive a corresponding control gate signal CG_1, CG_2 and CG_3, respectively.

[0030] Array 200 is programmed on a row-by-row basis in the described embodiment. While the first row of product term cells 201_1-202_1 is being programmed in the manner described above, control gate signals CG_2 and CG_3 for the other rows are all held at a voltage of about ½ V_{PP}, such that the associated product term cells 201_2-202_2 and 201_3-202_3 are not subjected to programming conditions.

[0031] After the first row of product term cells 201_1-202_1 has been programmed, the CG_1 signal is raised back to a voltage of ½ V_{PP}. The second row of product term cells 201_2-202_2 is then programmed in the manner described above, with control gate signals CG_1 and CG_3 being held at a voltage of about ½ V_{PP}, such that the associated product term cells 201_1-202_1 and 201_3-202_3 are not subjected to programming conditions.

[0032] After the second row of product term cells 201_2-202_2 has been programmed, the CG_2 signal is raised back to a voltage

of ½ V_{PP}. The third row of product term cells 201_2-202_2 is then programmed in the manner described above. After the third row of product term cells has been programmed, the $PBIT_{L1}$-$PBIT_{L2}$ and $PBIT_{R1}$-$PBIT_{R2}$ signals brought to the ground supply voltage. Then, the control gate signals CG_1-CG_3 are brought to the ground supply voltage. The $PBIT_{L1}$-$PBIT_{L2}$ and $PBIT_{R1}$-$PBIT_{R2}$ signals must be at the ground supply voltage before returning all of the control gate signals CG_1-CG_3 to the ground supply voltage to avoid mis-programming any cells.

[0033] After product term cell 100 has been erased/programmed, this product term cell is configured for normal operation. During normal operation, the V_{DD} terminal and the control gate terminal CG are coupled to receive the V_{DD} supply voltage (e.g., 1.8 Volts) and the $PBIT_L$ and $PBIT_R$ terminals are coupled to receive the ground supply voltage. Under these conditions, the logical operation of product term cell 100 depends on the programmed or erased state of the floating gates FG_L and FG_R. Table 1 below defines the manner in which the output signal OUT is provided in response to the input signals $Z_{IN}/Z_{IN\#}$ for the various programmed/erased states of floating gates FG_L and FG_R. In general, by setting the states of the floating gates appropriately, the product term cell 100 may be configured to provide one of a constant logic high, a constant logic low, Z_{IN}, or $Z_{IN\#}$ as the output signal OUT.

TABLE 1

FG_L	FG_R	Z_{IN}	$Z_{IN\#}$	OUT
ERASED	ERASED	0	1	1 (=1)
ERASED	ERASED	1	0	1 (=1)
ERASED	PROGRAMMED	0	1	1 ($=Z_{IN\#}$)
ERASED	PROGRAMMED	1	0	0 ($=Z_{IN\#}$)
PROGRAMMED	ERASED	0	1	0 ($=Z_{IN}$)
PROGRAMMED	ERASED	1	0	1 ($=Z_{IN}$)
PROGRAMMED	PROGRAMMED	0	1	0 (=0)
PROGRAMMED	PROGRAMMED	1	0	0 (=0)

[0034] When the floating gates FG_L and FG_R are both erased, both p-channel transistors 101 and 103 are in a conductive state, and both n-channel transistors 106 and 108 are in a non-conductive state. Since $Z_{IN\#}$ is the inverse of Z_{IN}, the $Z_{IN}/Z_{IN\#}$ signals always turn on one of the p-channel transistors 102 or 104, thereby coupling the output terminal 130 to the V_{DD} terminal. As a result, a logic high ("1") output signal OUT is provided, regardless of the state of the $Z_{IN}/Z_{IN\#}$ signals.

[0035] Conversely, when the floating gates FG_L and FG_R are both programmed, both n-channel transistors 106 and 108 are in a conductive state, and both p-channel transistors 101 and 103 are in a non-conductive state. Again, since $Z_{IN\#}$ is the inverse of Z_{IN}, the $Z_{IN}/Z_{IN\#}$ signals always turn on one of the n-channel transistors 105 or 107, thereby coupling the output terminal 130 to the ground voltage supply terminal. As a result, a logic low ("0") output signal OUT is provided, regardless of the state of the $Z_{IN}/Z_{IN\#}$ signals.

[0036] When the left floating gate FG_L is erased and the right floating gate FG_R is programmed, p-channel transistor 101 and n-channel transistor 106 are each in a conductive state, and p-channel transistor 103 and n-channel transistor 108 are

each in a non-conductive state. In this case, the product term cell is responsive to the Z_{IN} signal. Thus, if the Z_{IN} signal has a logic low state, then p-channel transistors 101 and 102 are both in a conductive state (and n-channel transistor 105 is in a non-conductive state), such that the output terminal 130 is pulled up to the V_{DD} supply voltage. Conversely, if the Z_{IN} signal has a logic high state, then n-channel transistors 105 and 106 are both in a conductive state (and p-channel transistor 102 is in a non-conductive state), such that the output terminal 130 is pulled down to the ground supply voltage. Thus, the output signal OUT is equal to the inverse of the Z_{IN} signal (or $Z_{IN\#}$).

[0037] When the right floating gate FG_R is erased and the left floating gate FG_L is programmed, p-channel transistor 103 and n-channel transistor 108 are each in a conductive state, and p-channel transistor 101 and n-channel transistor 106 are each in a non-conductive state. In this case, the product term cell is responsive to the $Z_{IN\#}$ signal. Thus, if the $Z_{IN\#}$ signal has a logic low state, then p-channel transistors 103 and 104 are both in a conductive state (and n-channel transistor 107 is in a non-conductive state), such that the output terminal 130 is pulled up to the V_{DD} supply voltage. Conversely, if the $Z_{IN\#}$ signal has a logic high state, then n-channel transistors 107 and 108 are both in a conductive state (and p-channel transistor 104 is in a non-conductive state), such that the output terminal 130 is pulled down to the ground supply voltage. Thus, the output signal OUT is equal to the inverse of the $Z_{IN\#}$ signal (or Z_{IN}).

[0038] Fig. 3 is a circuit diagram of a symmetrical product term cell 300 in accordance with another embodiment of the present invention. Because product term cell 300 (Fig. 3) is similar to product term cell 100 (Fig. 1), similar elements in

Figs. 1 and 3 are labeled with similar reference numbers. Thus, product term cell 300 includes high-voltage p-channel transistors 101-104, n-channel transistors 105-108, capacitors 111-112, and tunnel oxide capacitor elements 121-122. In addition, product term cell 300 includes left bit line 301, right bit line 302 and n-channel read transistor 303. The sources of n-channel transistors 106 and 108 are coupled to left bit line 301 and right bit line 302, respectively (rather than to the ground supply voltage terminal, as in pterm cell 100 of Fig. 1). N-channel read transistor 303 has a source coupled to the ground voltage supply terminal, a drain coupled to the output terminal 130 and a gate coupled to receive a read control signal (READ).

[0039] Product term cell 300 is erased and programmed in the same manner as product term cell 300. During erase and program operations, the LBIT and RBIT signals on left bit line 301 and right bit line 302 are held at the ground supply voltage, and the READ control signal is held at a logic low state, thereby turning off read transistor 303.

[0040] After product term cell 300 has been erased/programmed, this product term cell is configured for normal operation. During normal operation, the V_{DD} terminal and the control gate terminal CG are coupled to receive the V_{DD} supply voltage (e.g., 1.8 Volts) and the $PBIT_L$, $PBIT_R$, LBIT, RBIT and READ signals are held at the ground supply voltage. Under these conditions, the logical operation of product term cell 300 depends on the programmed or erased state of floating gates FG_L and FG_R. Product term cell 300 operates in accordance with Table 1 above (i.e., in the same manner as product term cell 100 of Fig. 1).

[0041] In addition, product term cell 300 allows for the state of its floating gates to be read. The programmed/erased

states of floating gates FG_L and FG_R of product term cell 300 can be read as follows. The Z_{IN}, $Z_{IN\#}$, READ and CG signals are held at the V_{DD} supply voltage, and the $PBIT_L$ and $PBIT_R$ signals are held at the ground supply voltage. The logic high Z_{IN} and $Z_{IN\#}$ signals turn on n-channel transistors 105 and 107, and turn off p-channel transistors 102 and 104. The logic high READ signal turns on read transistor 303, such that the ground supply voltage is applied to the drains of n-channel transistors 106 and 108. If left floating gate FG_L is programmed, then the V_{DD} supply voltage applied to the control gate terminal CG will cause n-channel transistor 108 to be in a conductive state. As a result, the right bit line 302 will be pulled down to the ground supply voltage. Similarly, if right floating gate FG_R is programmed, then the V_{DD} supply voltage applied to the control gate terminal CG will cause n-channel transistor 106 to be in a conductive state. As a result, the left bit line 301 will be pulled down to the ground supply voltage.

[0042] In contrast, if left floating gate FG_L is erased, then the V_{DD} supply voltage applied to the control gate terminal CG will not be sufficient to turn on n-channel transistor 108. As a result, the right bit line 302 remains floating (i.e., is not pulled down to the ground supply voltage). If right floating gate FG_R is erased, then the V_{DD} supply voltage applied to the control gate terminal CG will not be sufficient to turn on n-channel transistor 106. As a result, the left bit line 301 remains floating (i.e., is not pulled down to the ground supply voltage).

[0043] As is known in the art, conventional sense amplifier circuitry (not shown) may be coupled to the left and right bit lines 301 and 302 to sense the states of the LBIT and RBIT signals. A ground voltage state identifies a programmed state

of the associated floating gate, and a floating state identifies an erased state of the associated floating gate. For example, the left and right bit lines 301 and 302 may be pre-charged, and held at the pre-charge voltage by associated half-latch circuits (not shown). A programmed floating gate will result in the associated bit line being pulled down to ground, while an erased floating gate will result in the associated bit line remaining pulled up to the pre-charge voltage.

[0044] Having the Z_{IN} and $Z_{IN\#}$ signals at the V_{DD} supply voltage during the read operation turns off any possible current path through the p-channel transistors 101-104 of product term cell 300. One advantage of product term cell 300 is the ability to margin test the strength of the programmed floating gate n-channel transistors 106 and 108 by selecting different control gate voltages CG during a read operation. That is, the control gate voltage CG can be reduced during successive read operations to determine the minimum control gate voltage CG that will cause the sense amplifier to properly identify the programmed states of floating gate n-channel transistors 106 and 108.

[0045] Fig. 4 is a block diagram of a 2x2 array 400 of product term cells 401_1-401_2, 402_1-402_2 each of which is substantially identical to product term cell 300. Although a 2x2 array is illustrated, it is understood that this array can be expanded or contracted as necessary in view of the following teachings. In the illustrated embodiment, the product term cells 401_1-402_1 of the first column are commonly coupled to receive the $PBIT_{L1}$, $PBIT_{R1}$, $LBIT_1$ and $RBIT_1$ signals. Similarly, the product term cells 401_2-402_2 of the second column are commonly coupled to receive the $PBIT_{L2}$, $PBIT_{R2}$, $LBIT_2$ and $RBIT_2$ signals. Each row of product term cells 401_1-401_2

and 402_1-402_2 is coupled to receive a corresponding control gate signal CG_1 and CG_2, respectively, and a corresponding read control signal R_1 and R_2, respectively.

[0046] Array 400 is programmed on a row-by-row basis in the same manner described above for array 200. Note that the $LBIT_1$-$LBIT_2$, $RBIT_1$-$RBIT_2$ and R_1-R_2 signals are all held at the ground supply voltage during the programming operations.

[0047] Array 400 is also read on a row-by-row basis. For example, the first row of product term cells 401_1-401_2 is read as follows. The Z_{IN} and $Z_{IN\#}$ signals associated with each of product term cells 401_1-401_2 and the read control signal R_1 are activated high (V_{DD}) to read the first row. The Z_{IN} and $Z_{IN\#}$ signals associated with each of product term cells 402_1-402_2 and the read control signal R_2 are deactivated low (ground), since the second row is not being read. The control gate signal CG_1 is held at the V_{DD} supply voltage. The control gate signal CG_2 and the $PBIT_{L1}$-$PBIT_{L2}$ and $PBIT_{R1}$-$PBIT_{R2}$ signals are held at the ground supply voltage. Under these conditions, the contents of product term cells 401_1 and 401_2 can be read on bit lines $LBIT_1$-$RBIT_1$ and $LBIT_2$-$RBIT_2$ in the manner described above.

[0048] Although the invention has been described in connection with several embodiments, it is understood that this invention is not limited to the embodiments disclosed, but is capable of various modifications, which would be apparent to one of ordinary skill in the art. Thus, the present invention is only limited by the following claims.